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1. **Partially-parallel LDPC decoder based on high-efficiency message-passing algorithm**
Shimizu, K.; Ishikawa, T.; Togawa, N.; Ikenaga, T.; Goto, S.;
Computer Design, 2005. Proceedings. 2005 International Conference on
2-5 Oct. 2005 Page(s):503 - 510
IEEE CNF
2. **A 8-bit MCU design using a four-pipeline architecture**
Qing-Lan Lv; Ping Li;
Communications, Circuits and Systems and West Sino Expositions, IEEE 2002 International Conference on
Volume 2, 29 June-1 July 2002 Page(s):1462 - 1465 vol.2
IEEE CNF
3. **An architecture for multiresolution, focal, image analysis**
Burt, P.J.; van der Wal, G.;
Pattern Recognition, 1990. Proceedings., 10th International Conference on
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IEEE CNF
4. **A triangular systolic array for the discrete-time deconvolution**
Hussain, M.G.M.; Jaragh, M.;
Circuits and Systems, IEEE Transactions on
Volume 36, Issue 4, April 1989 Page(s):622 - 628
IEEE JNL
5. **A programmable concurrent video signal processor**
Chih-Chin Chen; Chein-Wei Jen;
Image Processing, 1996. Proceedings., International Conference on
Volume 1, 16-19 Sept. 1996 Page(s):1039 - 1042 vol.2
IEEE CNF
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Gregoret, F.; Intini, F.; Lavagno, L.; Passercne, R.; Reyneri, L.M.;
Parallel and Distributed Processing, 1996. PDP '96. Proceedings of the Fourth Euromicro Workshop on
24-26 Jan. 1996 Page(s):290 - 296
IEEE CNF
7. **A pyramid-based front-end processor for dynamic vision applications**
Burt, P.J.;
Proceedings of the IEEE
Volume 90, Issue 7, July 2002 Page(s):1188 - 1200
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8. **Fast Fourier transform processor based on low-power and area-efficient algorithm**
Jung-yeol Oh; Myoung-seob Lim;
Advanced System Integrated Circuits 2004. Proceedings of 2004 IEEE Asia-Pacific Conference on
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IEEE CNF
9. **An embedded processor core for consumer appliances with 2.8GFLOPS and 36M polygons/s FPU**
Arakawa, F.; Yoshinaga, T.; Hayashi, T.; Kiyoshige, Y.; Okada, T.; Nishibori, M.; Hiraoka, T.; Ozawa, M.; Kodama, T.; Irita, T.; Kamei, T.; Ishikawa, M.; Nitta, Y.; Nishii, O.; Hattori, T.;
Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International
15-19 Feb. 2004 Page(s):334 - 531 Vol.1

IEEE CNF

10. **High performance single chip dataflow processor**
Kuru, G.;
ASIC Conference and Exhibit, 1995., Proceedings of the Eighth Annual IEEE International
18-22 Sept. 1995 Page(s):346 - 349
IEEE CNF
11. **The bit-serial systolic back-projection engine (BSSBPE)**
Bayford, R.;
Application Specific Array Processors, 1990. Proceedings of the International Conference on
5-7 Sept. 1990 Page(s):43 - 54
IEEE CNF
12. **Video composition methods and their semantics**
Lin, H.-D.; Messerschmitt, D.G.;
Acoustics, Speech, and Signal Processing, 1991. ICASSP-91., 1991 International Conference on
14-17 April 1991 Page(s):2833 - 2836 vol.4
IEEE CNF
13. **An advanced dataflow processor architecture based on a multiple input node concept**
Kuru, G.; Deshmukh, R.G.;
Southeastcon '93, Proceedings., IEEE
4-7 April 1993 Page(s):8 p.
IEEE CNF
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Shousheng He; Torkelson, M.;
Signals, Systems, and Electronics, 1998. ISSSE 98. 1998 URSI International Symposium on
29 Sept.-2 Oct. 1998 Page(s):257 - 262
IEEE CNF
15. **A highly efficient AES cipher chip**
Chih-Pin Su; Tsung-Fu Lin; Chih-Tsun Huang; Cheng-Wen Wu;
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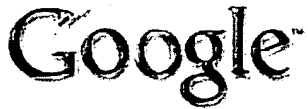
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sandpile.org -- IA-32 architecture -- Intel P5-core PeMo events

pipeline flushes due to wrong branch prediction, but resolved in WB-stage, occurrence ...

stall on MMX instruction write to E or M line, duration ...

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cycles per instruction. Clock cycle unpipelined ...

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How to Analyze **Pipeline Stalls** on 64-Bit Intel® **Architecture**. Challenge. Identify and categorize the causes of **pipeline stalls** for maximum performance on ...

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stalls, instruction set principles, **pipeline stall** cycles, ...

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High Performance Computer **Architecture**. Lecture 4. **Pipeline Hazards** ... Simplest

solution is to **stall** the **pipeline** upon detecting a branch ...

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Intel® NetBurst™ Architecture - Intel® Software Network

A classic **pipeline stall** occurs when the code requires a jump. ... the instruction set in the

EPIC **architecture** used in Intel's Itanium®-based processor was ...

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Exceptions may occur at different stages in **pipeline** (ie out of order): ... If any store prior to load is waiting for its address, **stall** load. ...

[www.cs.berkeley.edu/~culler/courses/cs252-s05/lectures/cs252s05-lec09-precise-](http://www.cs.berkeley.edu/~culler/courses/cs252-s05/lectures/cs252s05-lec09-precise-exceptions.ppt)

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How to Analyze Memory Accesses on 64-Bit Intel® Architecture

How to Analyze Memory Accesses on 64-Bit Intel® **Architecture** ... Determine what

memory accesses are causing EXE **pipeline stalls** accumulated by the ...

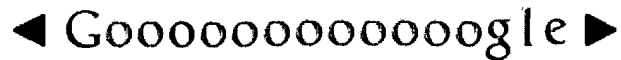
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Technical Note TN2087: PowerPC G5 Performance Primer

These stalls can be addressed by better code scheduling, loop unrolling and software ...

Due to the increased number of execution pipeline stages and the ...

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NeXT and Sun, SPIM simulator

Assume that for the **pipeline architecture**, a branch not taken incurs no penalty but a branch taken incurs a three cycle **stall**, and that data forwarding ...

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stall. 2. act. MeFoSyLoMa - 24 Mars 2006 - CTL-Property Transformations Along an ...

Applicable for the design of systems with **pipeline architecture** ...

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Control Reg. Datapath Stage. Nxt **Pipeline** Contr Reg. **Stall**. 1/27/2005 ...

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implementation of a subset of the Alpha **architecture**. ... when to **stall**. You can **stall** in the IF, ID or EX **pipeline** stages by setting the appropriate ...

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Pipeline CPI = Ideal **pipeline** CPI + Structural **stalls** + RAW **stalls** ... Basic (**stall** the **pipeline**); Predict-not-taken and predict-taken; Delayed branch and ...

www.cse.ohio-state.edu/~srini/775/Ch3.ppt - [Similar pages](#)

Differential Multithreading: Recapturing Pipeline Stall Cycles and ...

... a single issue **architecture**. dMT switches among multiple instruction streams in response to **pipeline stall** conditions but saves in flight instructions, ...

citeseer.ist.psu.edu/haskins00differential.html - 24k - [Cached](#) - [Similar pages](#)

David Davidian's Blog : Weblog

Processor **Architecture** Evolution and Chip Multi Threading ... The alternative was to have the complex **pipeline** either: **stall** on a cache miss, use a complex ...

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Resolve memory access **stalls** in the EXE **pipeline** stage on 64-Bit Intel **architecture**.

Memory access **stalls** occur when the data is not available in the caches ...

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timed bit-serial and fully interlocked **pipeline architecture**. The **architecture** is tailored to the ... signal in the **architecture**. "Block-stall" means that a ...

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10064597	6944749	150	07/29/2002	METHOD FOR QUICKLY DETERMINING LENGTH OF AN EXECUTION PACKAGE	KU, SHAN-CHYUN
10207829	Not Issued	61	07/31/2002	Method for improving instruction selection efficiency in a DSP/RISC compiler	KU, SHAN-CHYUN
10210075	Not Issued	161	08/02/2002	Decoding method for a variable-length instruction set	KU, SHAN-CHYUN
10377615	Not Issued	41	03/04/2003	Method of simulating computation instructions for an instruction set simulator	KU, SHAN-CHYUN
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